

ATTORNEY DOCKET  
1339-CA (P192 C1)

2

NO. PATENT  
U.S. 10/643,127

### Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

All claims currently being amended are shown with deleted text struckthrough or double bracketed and new text underlined. Additionally, the status of each claim is indicated in parenthetical expression following the claim number.

Claims 16-17, 28-35 remain.

Claims 16, 28, 33, and 34 are being amended.

Claims 26 and 37 are being added.

### WHAT IS CLAIMED IS:

16. (Currently Amended) A method of operating a switched capacitor integrator comprising the steps of:

    during a sampling phase selectively sampling a reference charge of a selected polarity onto an input plate of a reference capacitor in response to a control signal;

    during the sampling phase selectively sampling an input signal charge onto an input sampling capacitor;

    during a first period of an integration phase, transferring the sampled charges from the reference and input sampling capacitors to a common node; and

    during a second period of the integration phase following the first period of the integration phase, coupling the common node and the integration capacitor to transfer substantially all of the sampled charges from the common node to an integration capacitor.

17. (Original) The method of Claim 16 further comprising the step of generating the control signal during an integration phase preceding said step of sampling the reference voltage.

021615.500007 Dallas 1759726.1

ATTORNEY DOCKET  
1339-CA (P192 C1)

3

NO. PATENT  
U.S. 10/643,127

28. (Currently Amended) A method of operating a switched capacitor integrator comprising the steps of:

during a sampling phase selectively sampling a charge of a selected polarity onto a capacitor in response to a control signal;

during the sampling phase selectively sampling a charge onto another capacitor;

during a first period of an integration phase, transferring the sampled charges from the capacitor and the another capacitor to a common node to generate a summed charge at the common node; and

during a second period of the integration phase following the first period of the integration phase, coupling the common node and the integration capacitor to transfer substantially all of the summed charge from the common node to an integration capacitor.

29. (Original) The method of Claim 28 further comprising the step of generating the control signal during an integration phase preceding said step of sampling the reference voltage.

30. (Original) The method of Claim 28 wherein:

selectively sampling a charge onto the capacitor comprises selectively sampling a charge of a selected polarity from a reference signal source; and

selectively sampling a charge onto the another capacitor comprises selectively sampling a charge of a selected polarity from the reference signal source.

31. (Original) The method of Claim 30 further comprising:

during the sampling phase, selectively sampling a charge from an input signal source onto an input sampling capacitor; and

during the first period of the integration phase, transferring the charge on the input sampling capacitor to the summing node for summing with the charges from the capacitor and the another capacitor.

021615.500007 Dallas 1759726.1

ATTORNEY DOCKET  
1339-CA (P192 C1)

4

NO. PATENT  
U.S. 10/643,127

32. (Original) The method of Claim 28 wherein:  
selectively sampling a charge onto the capacitor comprises selectively sampling  
a charge of a selected polarity from a reference signal source; and  
selectively sampling a charge onto the another capacitor comprises selectively  
sampling a charge of a selected polarity from an input signal source.

33. (Currently Amended) An integrator stage for use in a delta sigma modulator  
comprising:  
an operational amplifier;  
an integration capacitor coupling an output of the operational amplifier and a  
summing node to an input of the operational amplifier;  
first and second feedback paths each including switching circuitry for selectively  
sampling reference charges of selected polarities onto corresponding first and second  
capacitors during a sampling phase;  
switching circuitry for summing during a first period of an integration phase the  
charge sampled onto the first and second capacitors onto a common node; and  
a switch for selectively coupling a substantial portion of the summed charge on  
the common node to the integration capacitor during a second period of the integration  
phase, the second period of the integration phase following the first period of the  
integration phase.

34. (Currently Amended) The integrator stage of Claim 33 further comprising  
switching circuitry for sampling a charge from an input signal source onto another  
[[a third]] capacitor during the sampling phase and switching circuitry for summing the  
charge sampled on the third capacitor onto the summing node during the first period of  
the integration phase.

35. (Original) The integrator stage of Claim 33 wherein the delta-sigma  
modulator forms a portion of a analog to digital converter.

021615.500007 Dallas 1759726.1

ATTORNEY DOCKET  
1339-CA (P192 C1)

5

NO. PATENT  
U.S. 10/643,127

36. (New)           The method of Claim 16 further comprising:  
                  during a first period of another integration phase, transferring the sampled charges from the reference and input sampling capacitors to the common node; and  
                  during a second period of the another integration phase following the first period of the another integration phase, coupling the common node and the integration capacitor to transferring substantially all of the sampled charges from the common node to the integration capacitor.

37. (New)           The integrator stage of Claim 33 wherein:  
                  the first and second feedback paths selectively sample reference charges of selected polarities onto the corresponding first and second capacitors during another sampling phase;  
                  the switching circuitry for summing sums during a first period of another integration phase the charge sampled onto the first and second capacitors onto a common node during the another sampling phase; and  
                  the switch for selectively coupling couples a substantial portion of the summed charge on the common node to the integration capacitor during a second period of the another integration phase, the second period of the another integration phase following the first period of the integration phase.

021615.500007 Dallas 1759726.1